Design of an Efficient Parallel Comparator Architecture for Low Power Delay Product

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Abstract. *A binary comparator architecture is proposed in this work for static logic to achieve both low-power and high-performance operations. It also presents a detailed timing performance and power analysis of various state-of-the-art comparator designs. The main advantages of this design are its high speed and power efficiency maintained over a wide range of operands size, which is useful at low-input data activity environments. The proposed circuit design uses minimum fan-in and fan-out logic gates for achieving high speed and low power dissipation. Utilizing a 2-bit binary comparator circuit with minimum fan-in and fan-out of logic gates (NAND-NOR), the architecture of a parallel binary comparator is proposed for higher input operands by using a low radix multiplexer and priority encoder. Further, to decrease the size of the multiplexer and priority encoder by two times, a general architecture is also proposed by using a 4-bit binary comparator to reduce its complexity. The proposed circuits are optimized in terms of the power consumption and delay, which are due to low load capacitance, low leakages, and reduced dynamic power dissipation. Each of the proposed circuits has its own merits in terms of speed, power consumption, Power-Delay Product (PDP). Its synthesis is done on 180 nm as well as 90 nm CMOS technology using the Cadence tool. The physical layout of the proposed architecture using a 90 nm CMOS process (GPDK process) is also obtained.*

Keywords

Binary comparator, delay, power dissipation, PDP, physical layout design, VLSI.

1. Introduction

In modern processors or digital systems, a binary comparator is one of the basic and essential parts. It is heavily used in various fundamental processes of computing and communication, including sorting of string, random number generation, and searching of data [1], [2], [3] and [4]. The sorting operation includes various comparison steps to arrange a large amount of data in ascending or descending order. The algorithm for object reorganization uses the comparisons on its key point localization stage [5]. A data-intensive application such as 3D graphics and image processing is also widely used by comparators [6]. The use of a binary comparator circuit is also observed in a Digital Signal Processor (DSP) [7], application-oriented processors, such as media processors [8], vision processors [7], [8], [9] and [10], etc. In modern ICs design, a binary comparator circuit plays the key component in Design For Testability (DFT), such as Built-In Self-Test (BIST), the design of signature analyzer, and parallel testing [11] for the Circuit Under Test (CUT). For the next-generation communication systems, Multiple-Input-Multiple-Output (MIMO) technology has required high performance and low power binary comparator systems for decoding of the MIMO algorithms that required extensive comparisons of binary numbers [12]. For these applications in VLSI circuits, higher operand comparator designs are essential nowadays. Apart from that, a comparison between two operands is a critical operation in high-speed demand for supercomputing. Therefore, high speed and low power consumable binary comparator is a primary requirement in modern VLSI design, and it should be optimized carefully to develop fast and power-efficient electronic systems. In the last decade, the design of low

power, high speed, and area-efficient binary comparators have received several design challenges [13]. Power consumption and computational delay are important factors in the design of digital systems. High computational delay and high switching activity will degrade the circuit performance resulting in high power consumption and lower circuit reliability, it causes shorten the circuit's lifetime or increases its failure rate [14].

To design a binary comparator, the Manchester chain adder is used to fulfill the compare operation [15]. The drawback of the circuit is a slower response and high power dissipation due to circuit complexity, and it is not suitable for a high radix binary comparator. To increase the speed, a comparator with a high-speed adder is proposed in [16]. A low power binary comparator architecture was proposed in [17]. It is designed by rippling from MSB to LSB of input operands and minimize the power dissipation by dynamically eliminating unnecessary computations. A digital comparator using different techniques such as half adder and multiplexer is proposed in [18]. A 12-bit digital comparator using multiplexer for high-speed application is proposed in [19]. A 64-bit comparator based on two-phase clocked dynamic CMOS logic was designed with the concept of the pipelining structure of dynamic CMOS logic [20]. In [21], a single clock two-phase binary comparator is studied. A binary comparator using different types of priority encoder and multiplexer was presented in [22] and [23]. A Floating Gate MOSFET (FGMOS) based 4-bit binary comparator was proposed in [24]. The above literature of binary comparator architecture uses dynamic CMOS logic to achieve high-performance operations, but it consumes more power due to high data activity factors.

Recently, a tree-based structure of binary comparator was proposed in [25], [26], [27], [28], [29], [30] and [31] which uses the concept of carry merge tree of parallel prefix adder. A parallel binary comparator based on the prefix tree and XOR-XNOR circuit is proposed in [32]. Its binary comparator design includes the following modules: compare, pre-encoder, compression terminates, and decision module. The drawback of this architecture is required large fan-in and fan-out logic gates, which increases with the input operand size of the comparator circuit. Therefore, computational delay and power dissipation of this architecture exponentially increases with the size of the operand of a binary comparator. In CMOS circuits with high fan-in and fan-out logic gates, the circuit performance degrades effectively, i.e. circuit shows higher propagation delay and higher power dissipation.

In this brief, a novel architecture for an efficient binary comparator circuit with minimum fan-in and fan-out logic gates is designed for static logic to achieve both low-power and high-performance operation, particularly at low-input data activity environments. Utilizing the concept of 2-bit comparator [33], a general 2N-bit parallel architecture of the comparator system is proposed for higher input operands with low radix multiplexer and priority encoder to achieve the minimum dynamic power dissipation with high operating speed due to low-input data activity environments. Further, to decrease the size of the multiplexer and priority encoder by two times, another 2N-bit parallel binary comparator is proposed using a 4-bit comparator, low radix multiplexer, and priority encoder. A 4-bit binary comparator is designed with the help of an elementary 2-bit comparator. The comparator circuits are simulated using 180-nm as well as 90-nm CMOS technology. The remaining brief is organized as follows. In Sec. 2. the proposed design of elementary 2-bit binary comparator is discussed. Section 3. presents the proposed general structures of the parallel 2N-bit binary comparator. Section 4. discusses the area and time complexity proposed and the existing binary comparator. Section 5. presents the result and discussion. Finally, Sec. 6. concludes the work.

2. Elementary 2-bit Binary Comparator

2.1. Basic Design Principle

Comparison of a 2-bit binary number (A_1A_0) and (B_1B_0) can be realized by following Boolean expression for Less (L), Greater (G), and Equal (E) signal:

$$G = A_1E_1 + X_1A_0E_0, \tag{1}$$

$$E = X_1X_0, \tag{2}$$

$$L = \overline{E+G}, \tag{3}$$

where $X = AB + \overline{A} \cdot \overline{B}$ and $E = \overline{A}B + A\overline{B}$.

Equation (1), Eq. (2) and Eq. (3) show the Boolean expression for the comparator's output [32]. The gate-level architecture of binary comparator, from above equations, has numerous weaknesses such as fan-in of logic-gates is directly proportional to the input operand size of the binary comparator, causes high power dissipation, and large propagation delay. It is designed by AND-OR logic gates, thus increasing the delay and reducing packing density of the chip as compared with CMOS based NAND-NOR logic gate. In Eq. (3), Signal 'L' is given by $(\overline{E+G})$. It depends on an equal and greater output signal so that the overall delay performance of the binary comparator circuit is increased.

To enhance the performance, *Gupta and Chauhan* proposed a 2-bit elementary structure of binary comparator by re-design techniques [33] that offer

independent fan-in of logic gates, and it is free from AND-OR logic gates that convert entire logic into NOR and NAND gates except XOR-XNOR logic gates. The boolean expression for the proposed 2-bit binary comparator is given by Eq. (4), Eq. (5) and Eq. (6) for 'L', 'G' and 'E' signal:

$$E = \overline{E_1 + E_0}, \tag{4}$$

$$G = \overline{(\overline{A_1}\overline{B_1})} \cdot \overline{((\overline{A_0}\overline{B_0}) + E_1)}, \tag{5}$$

$$L = \overline{(\overline{A_1}B_1)} \cdot \overline{((\overline{A_0}B_0) + E_1)}. \tag{6}$$

Figure 1 presents the proposed 2-bit binary comparator architecture with minimum fan-in (2-input) logic gate (NAND-NOR), which is designed by Eq. (4), Eq. (5) and Eq. (6). It is generating all outputs independently. All drawback of the comparator circuit [32] is compensated by the proposed binary comparator. So that the proposed comparator circuit can be efficient in terms of performance for digital comparison of binary operands.

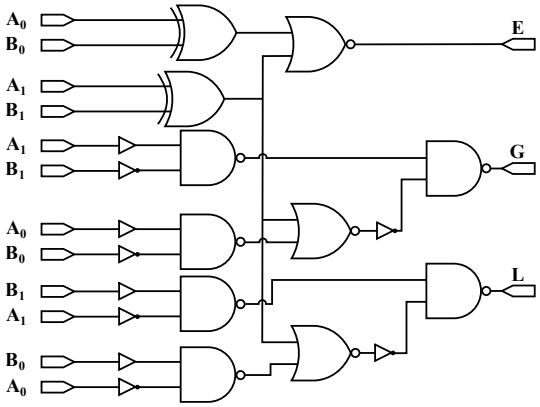


Fig. 1: Gate level schematics of 2-bit binary comparator [33].

3. The General Structure of The Proposed Binary Comparator

In the previous section, we proposed an elementary 2-bit high-performance binary comparator. Now in this section, we propose a generalized model for the binary comparator to compare high radix binary operands by utilizing the proposed 2-bit comparator circuit.

We consider 2N-bit input operands A and B, each operand will be divided into 2-bit input data from LSB to MSB and becomes a separate input of the individual 2-bit binary comparator. To identify the greater or less for individual input data, perform the logic OR operation with L and G signal as shown in Eq. (7). The output of each OR gate $(P_{N-1}, P_{N-2}, \ldots, P_1, P_0)$ becomes an input of priority encoder that identifies the first logic one from MSB to LSB of input data of priority encoder. The output of the priority encoder is given by $(Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0)$, where R is equal to $\log_2 N$. Once we find the first logic one from MSB to LSB of priority encoder inputs, we use the multiplexers of size N into 1 to find 2-bit data from input operands (A and B) corresponding to the first logic one. In the proposed architecture, four multiplexers have been used and the select line is controlled by an output signal of the priority encoder $(Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0)$. By using a multiplexer, we find the 2-bit inputs for the comparator i.e. (M_1, M_0) and (N_1, N_0) corresponding input operands A and B as given in Eq. (8), Eq. (9), Eq. (10) and Eq. (11). Finally, data M and N are an input of the 2-bit comparator and its output G and L becomes a final output for greater and less signal of proposed 2N-bit binary comparator architecture, it is given by Eq. (12) and Eq. (13). When both input operands A and B are equal, then the priority encoder's output becomes zero. Therefore, the equal signal is given by the NOR logic of the priority encoder's input as given in Eq. (14). Figure 2, Fig. 3 and Fig. 4 show the proposed 2N-bit parallel binary comparator architecture.

$$P_n = L_n + G_n, \tag{7}$$

where $n = 0$ to $N - 1$.

$$\begin{gathered} M_1 = A_1 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + A_3 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + A_{2N-3} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + A_{2N-1} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \end{gathered} \tag{8}$$

$$\begin{gathered} M_0 = A_0 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + A_2 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + A_{2N-4} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + A_{2N-2} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \end{gathered} \tag{9}$$

$$\begin{gathered} N_1 = B_1 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + B_3 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + B_{2N-3} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + B_{2N-1} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \end{gathered} \tag{10}$$

$$\begin{gathered} N_0 = B_0 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + B_2 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + B_{2N-4} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + B_{2N-2} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \end{gathered} \tag{11}$$

$$G = \overline{(\overline{M_1}\overline{N_1})} \cdot \overline{((\overline{M_0}\overline{N_0}) + \overline{M_1}N_1 + M_1\overline{N_1})}. \tag{12}$$

$$L = \overline{(\overline{M_1}N_1)} \cdot \overline{((\overline{M_0}N_0) + \overline{M_1}N_1 + M_1\overline{N_1})}. \tag{13}$$

$$E = \overline{E_{R-1} + E_{R-2} + \cdots + E_1 + E_0}. \tag{14}$$

The proposed general architecture for the comparator is shown in Fig. 2. We can observe that the size of the multiplexer and priority encoder are directly proportional to the size of the comparator along with

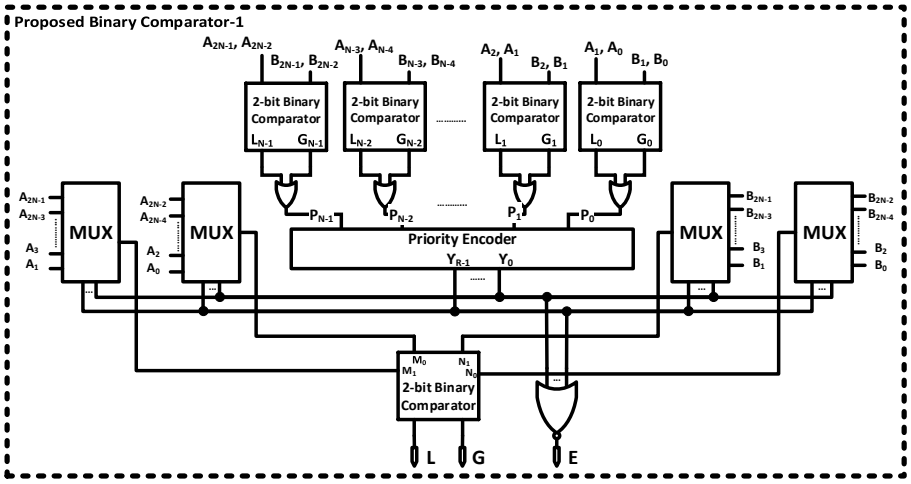


Fig. 2: Proposed architecture-1 for 2N-bit binary comparator system using a 2-bit elementary binary comparator.

the size of an elementary 2-bit comparator. To decrease the size complexity or radix of multiplexer and priority encoder, we can increase the size of elementary comparators, which is used to design the parallel architecture of binary comparator.

Figure 3 shows the 4-bit binary comparator. It is designed by using two proposed 2-bit elementary comparators, i.e. MSB and LSB comparator, inputs operands of the MSB comparator are A[1:0] and B[1:0]. Similarly, the inputs of the LSB comparator are A[3:2] and B[3:2]. Their output is (E_M, G_M, L_M) for MSB comparator and (E_L, G_L, L_L) for LSB comparator. And its logic gates connection is described by Eq. (15), Eq. (16) and Eq. (17).

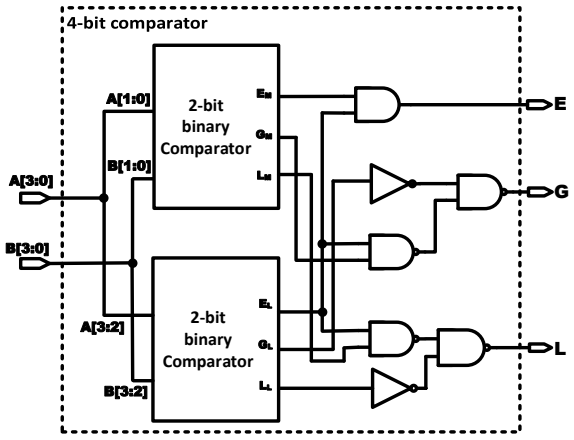


Fig. 3: The architecture for 4-bit binary comparator using a 2-bit elementary binary comparator.

$$E = E_M \cdot E_L. \tag{15}$$

$$G = \overline{\overline{G_L}(E_L \cdot G_M)}. \tag{16}$$

$$L = \overline{\overline{L_L}(E_L \cdot L_M)}. \tag{17}$$

To design the general architecture of binary comparator using 4-bit elementary comparator, i.e. shown in Fig. 4, we consider 2N-bit input operands A and B, each operand will be divided into 4-bit input data from LSB to MSB and become a separate input of the individual 4-bit binary comparator. To identify the greater or less for individual input data, perform the logic OR operation with L and G signal as shown in Eq. (18). The output of each OR gate $(P_{\frac{N}{2}-1}, P_{\frac{N}{2}-2}, \ldots, P_1, P_0)$ becomes an input of priority encoder, that is identified the first logic one from MSB to LSB of input data of priority encoder. The output of the priority encoder is given by $(Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0)$, where R is equal to $\log_2 \frac{N}{2}$. Once we find the first logic one from MSB to LSB of priority encoder inputs, we use the multiplexers of size $\frac{N}{2}$ into 1, to find 4-bit data from input operands (A and B) corresponding first logic one. In the proposed architecture, eight multiplexers are used and its select line is controlled by the output signal of the priority encoder $(Y_{R-1}, Y_{R-2}, \ldots, Y_1, Y_0)$. By using a multiplexer, we find the 4-bit inputs for the comparator, i.e. (M_3, M_2, M_1, M_0) and (N_3, N_2, N_1, N_0) corresponding input operands A and B, as given in Eq. (19),Eq. (20), Eq. (21), Eq. (22), Eq. (23), Eq. (24), Eq. (25) and Eq. (26). Finally, data M and N are an input of the 4-bit comparator, and its output G and L become a final output for greater and less signal of proposed 2N-bit binary comparator architecture. When both input operands A and B are equal, then the priority encoder's output becomes zero. Therefore, the equal signal is given by the NOR logic of the priority encoder's input as given in Eq. (14).

$$P_n = L_n + G_n, \tag{18}$$

where $n = 0$ to $\frac{N}{2} - 1$.

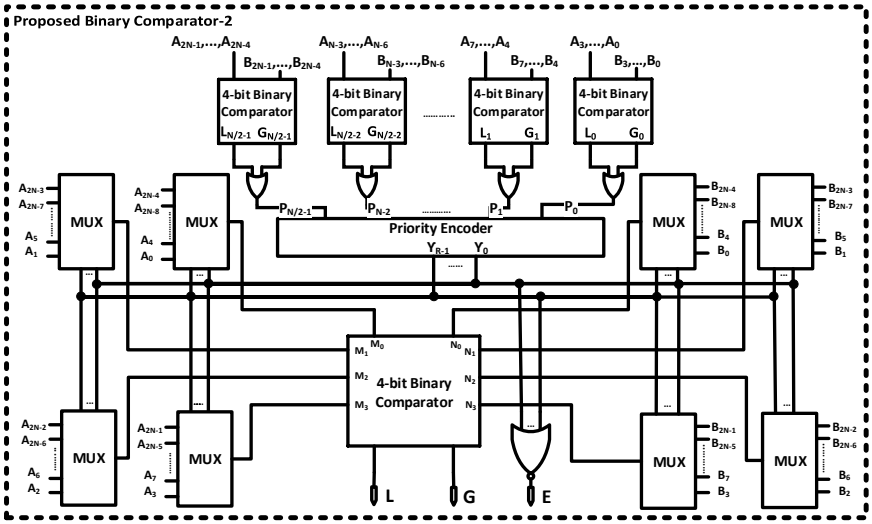


Fig. 4: Proposed architecture-2 for 2N-bit binary comparator architecture using a 4-bit binary comparator.

$$M_3 = A_3 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + A_7 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + A_{2N-5} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + A_{2N-1} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \tag{19}$$

$$M_2 = A_2 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + A_6 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + A_{2N-6} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + A_{2N-2} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \tag{20}$$

$$M_1 = A_1 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + A_5 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + A_{2N-7} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + A_{2N-3} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \tag{21}$$

$$M_0 = A_0 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + A_4 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + A_{2N-8} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + A_{2N-4} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \tag{22}$$

$$N_3 = B_3 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + B_7 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + B_{2N-5} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + B_{2N-1} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \tag{23}$$

$$N_2 = B_2 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + B_6 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + B_{2N-6} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + B_{2N-2} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \tag{24}$$

$$N_1 = B_1 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + B_5 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + B_{2N-7} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + B_{2N-3} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \tag{25}$$

$$N_0 = B_0 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot \overline{Y}_0) + \\ + B_4 \cdot (\overline{Y}_{R-1} \cdot \overline{Y}_{R-2} \ldots \overline{Y}_1 \cdot Y_0) + \cdots + \\ + B_{2N-8} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot \overline{Y}_0) + \\ + B_{2N-4} \cdot (Y_{R-1} \cdot Y_{R-2} \ldots Y_1 \cdot Y_0). \tag{26}$$

4. Timing and Area Complexity of Binary Comparator

This section discusses the area and timing complexity of the proposed architecture of two different binary comparators. The first architecture is a design by using a 2-bit elementary comparator, priority encoder, and multiplexers. Its maximum critical path delay is contributed by two 2-bit elementary comparators, $\frac{n}{2} \cdot 1$ multiplexer, $N \cdot \log_2 N$ priority encoder and 2-input OR gate. While in the second proposed architecture of 2N-bit binary comparator, critical path delay is contributed by two 4-bit elementary comparators, $\frac{n}{4} \cdot 1$ multiplexer, $\frac{N}{2} \cdot \log_2 \frac{N}{2}$ priority encoder and 2-input OR gate. The first proposed architecture of binary comparator utilizes the area of $(N+1)$ number of the 2-bit binary comparator, four $\frac{n}{2} \cdot 1$ multiplexer, $N \cdot \log_2 N$ priority encoder, N number of two-input OR gate and $\log_2 N$-input NOR gates. The second proposed architecture utilizes the area of $(\frac{N}{2}+1)$ number of the 4-bit binary comparator, four $\frac{n}{4} \cdot 1$ multiplexer, $\frac{N}{2} \cdot \log_2 N$ priority encoder, $\frac{N}{2}$ number of two-input OR gate and $\log_2 \frac{N}{2}$ inputs NOR gate. Table 1 presents the area and time complexity of proposed architectures of comparator circuits and compares with existing literature of binary comparators [32]. Here $A_{2\frac{i}{p}bc}$ and $T_{2\frac{i}{p}bc}$ represent the area and critical path delay of the 2-bit binary comparator. $A_{4\frac{i}{p}bc}$ and $T_{4\frac{i}{p}bc}$ represents the area and delay of the 4-bit binary comparator. $T_{\frac{N}{2}\frac{i}{p}mux}$, $T_{\frac{N}{4}\frac{i}{p}mux}$, $A_{\frac{N}{2}\frac{i}{p}mux}$, $A_{\frac{N}{4}\frac{i}{p}mux}$ are the timing and area complexity of $\frac{n}{2} \cdot 1$ and $\frac{n}{4} \cdot 1$ bit Multiplexer, respectively. $T_{N\frac{i}{p}pe}$, $T_{\frac{N}{2}\frac{i}{p}pe}$, $A_{N\frac{i}{p}pe}$, $A_{\frac{N}{2}\frac{i}{p}pe}$ represent the critical path delay and area complexity of N and $\frac{N}{2}$-bit priority encoder, respectively.

Tab. 1: Timing and area complexity of proposed and existing 2N-bit comparators.

Method	Timing complexity (Critical path)	Area complexity
Structure-1 [32]	$T_{2\frac{i}{p}xor} + T_{2N\frac{i}{p}and} + T_{not} +$ $+T_{2N\frac{i}{p}nand} + T_{\frac{N}{2}\frac{i}{p}nor} + T_{2\frac{i}{p}nor}$	$2N \cdot A_{2\frac{i}{p}xor} + (A_{2\frac{i}{p}and} + A_{3\frac{i}{p}and} + \cdots + A_{2N\frac{i}{p}and}) +$ $+2N \cdot A_{not} + \frac{N}{2} \cdot A_{4\frac{i}{p}nand} + \frac{N}{2} \cdot A_{4\frac{i}{p}nor} +$ $+A_{\frac{N}{2}\frac{i}{p}nor} + A_{\frac{N}{2}\frac{i}{p}and} + A_{2\frac{i}{p}nor}$
Structure-2 [32]	$T_{2\frac{i}{p}\frac{xor}{xnor}} + T_{2N\frac{i}{p}nand} +$ $+T_{2N\frac{i}{p}nor} + T_{\frac{N}{2}\frac{i}{p}and} + T_{2\frac{i}{p}nor}$	$2N \cdot A_{\frac{xor}{xnor}} + (A_{2\frac{i}{p}nand} + A_{3\frac{i}{p}nand} + \cdots + A_{2N\frac{i}{p}nand})$ $+\frac{N}{2} \cdot A_{4\frac{i}{p}and} + \frac{N}{2} \cdot A_{4\frac{i}{p}nor} + 2 \cdot A_{\frac{N}{2}\frac{i}{p}and} + A_{2\frac{i}{p}nor}$
Proposed 1	$2 \cdot T_{2\frac{i}{p}bc} + T_{\frac{N}{2}\frac{i}{p}mux} + T_{N\frac{i}{P}pe} + T_{or}$	$(N+1) \cdot A_{2\frac{i}{p}bc} + 4 \cdot A_{\frac{N}{2}\frac{i}{p}mux} + A_{N\frac{i}{p}pe} + A_{xor} + N \cdot A_{2\frac{i}{p}or}$
Proposed 2	$2 \cdot T_{4\frac{i}{p}bc} + T_{\frac{N}{4}\frac{i}{p}mux} + T_{\frac{N}{2}\frac{i}{p}pe} + T_{2\frac{i}{p}or}$	$(\frac{N}{2}+1) \cdot A_{4\frac{i}{p}bc} + 8 \cdot A_{\frac{N}{4}\frac{i}{p}mux} + A_{\frac{N}{2}\frac{i}{p}pe} + A_{xor} + \frac{N}{2} \cdot A_{2\frac{i}{p}or}$

Tab. 2: Simulation results of proposed and existing binary comparator circuits.

Reference	Technology	Size (bit)	Delay (ns)	Power dissipation (μW)	PDP (10^{-15} J)	Chip area (μm^2)
Ref. [25]	180-nm	16	0.778	1714.81	1333.745	864.419
		32	0.912	3098.13	2826.052	1710.393
		64	1.181	5073.24	5991.446	3418.417
Ref. [32] Structure-1	180-nm	16	0.381	1526.91	580.867	667.494
		32	0.512	2620.25	1340.861	1317.548
		64	0.685	3979.90	2723.406	2624.689
Ref. [32] Structure-2	180-nm	16	0.424	1349.38	572.245	488.654
		32	0.579	2444.19	1415.430	932.740
		64	0.889	3676.61	3267.808	1915.356
Proposed 1	180-nm	16	0.4053	1071.825	434.4106725	853.22175
		32	0.679	1909.91	1296.82889	1631.4435
		64	0.7287	3476.96	2533.660752	3135.33975
Proposed 2	180-nm	16	0.39655	852.035	337.8744793	716.00775
		32	0.4613	1591.23	734.034399	1454.46825
		64	0.7805	3049.47	2380.111335	2876.50425
Proposed 1	90-nm	16	0.1743	342.395	59.6794485	280.43175
		32	0.23065	657.045	151.5474293	566.5395
		64	0.336	1561.16	524.54976	1133.64675
Proposed 2	90-nm	16	0.2135	295.895	63.1735825	232.74675
		32	0.24465	517.39	126.5794635	477.41475
		64	0.3864	1090.115	421.220436	946.314

Tab. 3: Simulation and reported results for various comparator designs.

Reference	Technology	Bit size	Transistor count/chip μm^2	Total power dissipation (mW)	Delay (ns)	PDP (10^{-12} J)	Remarks
Ref. [17]	0.18 μm	24	624	5.23	4.16	21.757	Very slow
Ref. [23]	0.18 μm	32	964	2.53	1.12	2.834	Dynamic clock is heavily loaded with gated number of transistors
Ref. [34]	0.35 μm	64	2456	17.54	1.93	33.852	High energy consumption
Ref. [25]	0.18 μm	64	3418	5.073	1.181	5.991	High power dissipation
Ref. [32]	0.18 μm	64	1915.356	3.68	0.889	3.272	Achieving fast speed but high power dissipation
Proposed 1	0.18 μm	64	3135.339	3.476	0.7287	2.534	High speed with less power dissipation
Proposed 2	0.18 μm	64	2876.504	3.0495	0.7805	2.380	High speed with less power dissipation
Proposed 1	0.09 μm	64	1133.647	1.5612	0.336	0.525	High speed with less power dissipation
Proposed 2	0.09 μm	64	946.314	1.0901	0.3864	0.421	High speed with less power dissipation

5. Result and Discussion

The proposed binary comparator architectures with different operands sizes (16, 32, and 64-bit) are evaluated using a Cadence tool. For synthesis, we used 180-nm as well as 90-nm CMOS technology. Table 2 presents the synthesis results in terms of delay, total power dissipation, and Power-Delay-Product to measure the performance of the proposed design concerning other candidate designs. Table 3 represents the detailed analysis of the proposed and existing architecture of binary comparator and discusses their advantages and disadvantages in terms of low power

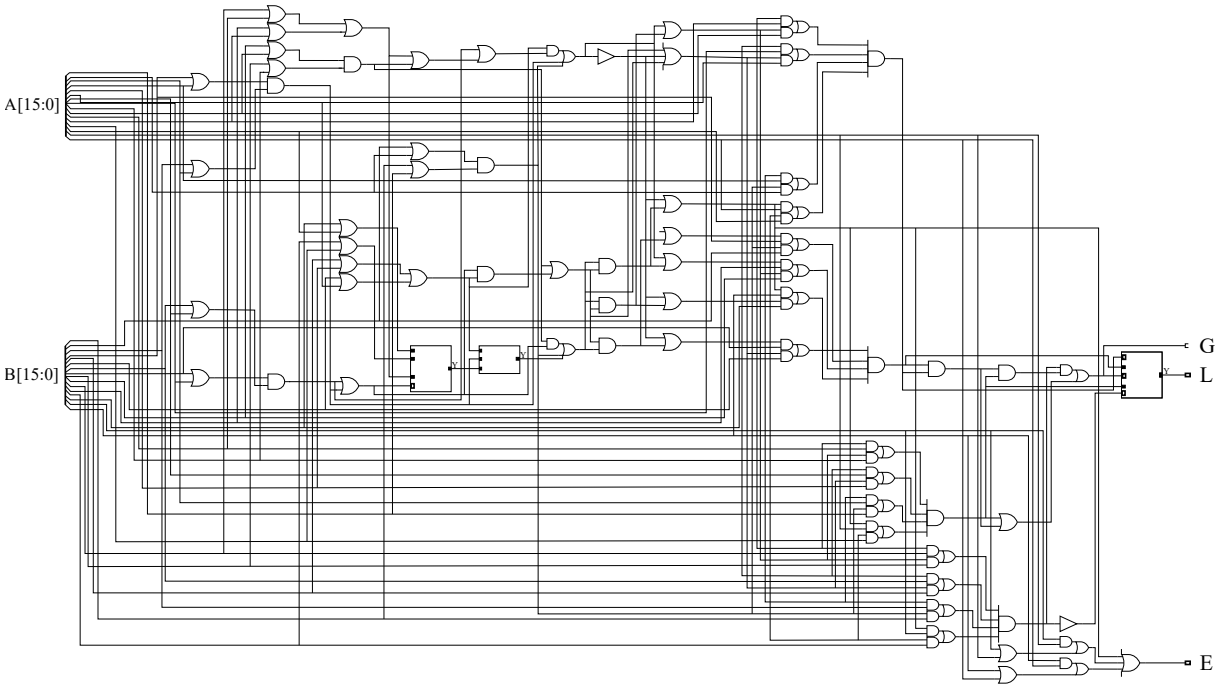


Fig. 5: RTL schematics of proposed 16-bit binary comparator using a 2-bit elementary comparator.

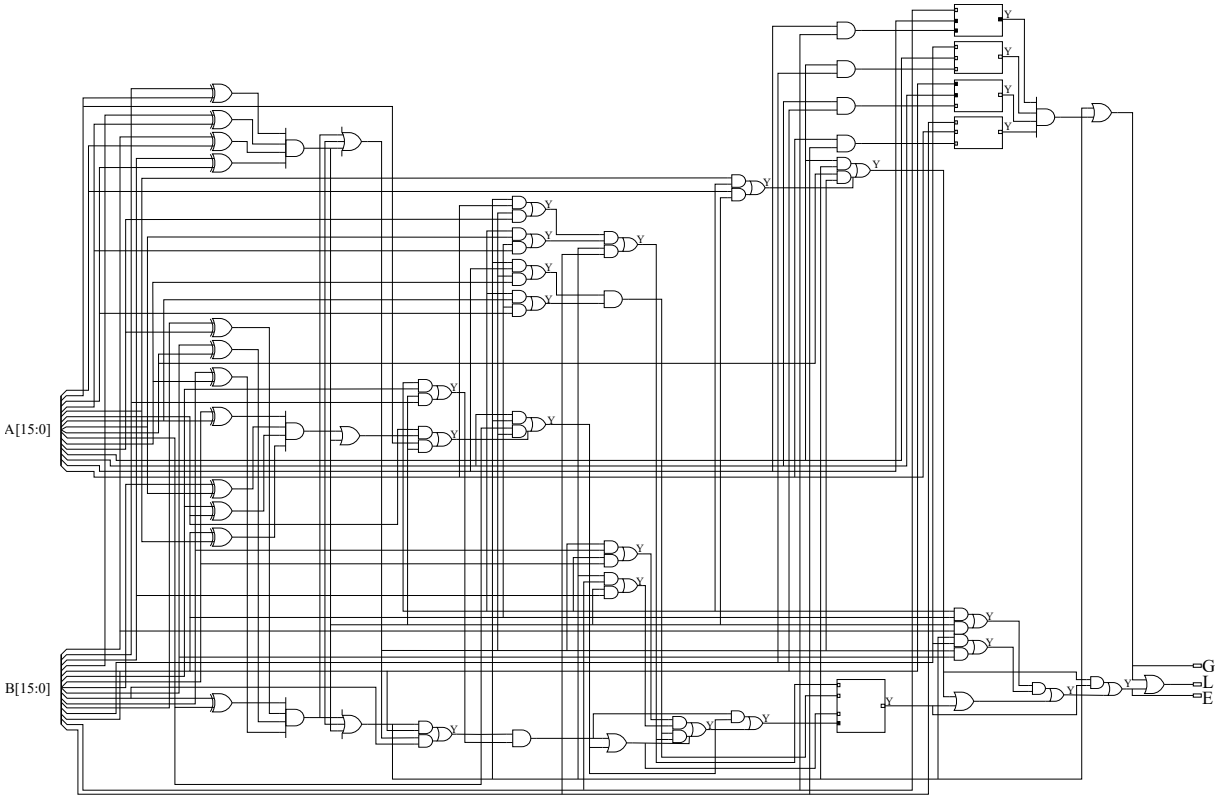


Fig. 6: RTL schematics of proposed 16-bit binary comparator using a 4-bit elementary comparator.

and high-performance applications. The PDP will be calculated by multiplying the critical path delay with the power dissipation of the circuit. The RTL schematics of proposed binary comparator architectures ($n = 16$) are shown in Fig. 5 and Fig. 6. Figure 7 and Fig. 8 show the physical layout design of proposed ($n = 16$) binary comparator architectures using a 90-nm CMOS process (90-nm GPDK). The simulation waveform of proposed architecture 1 and 2 with

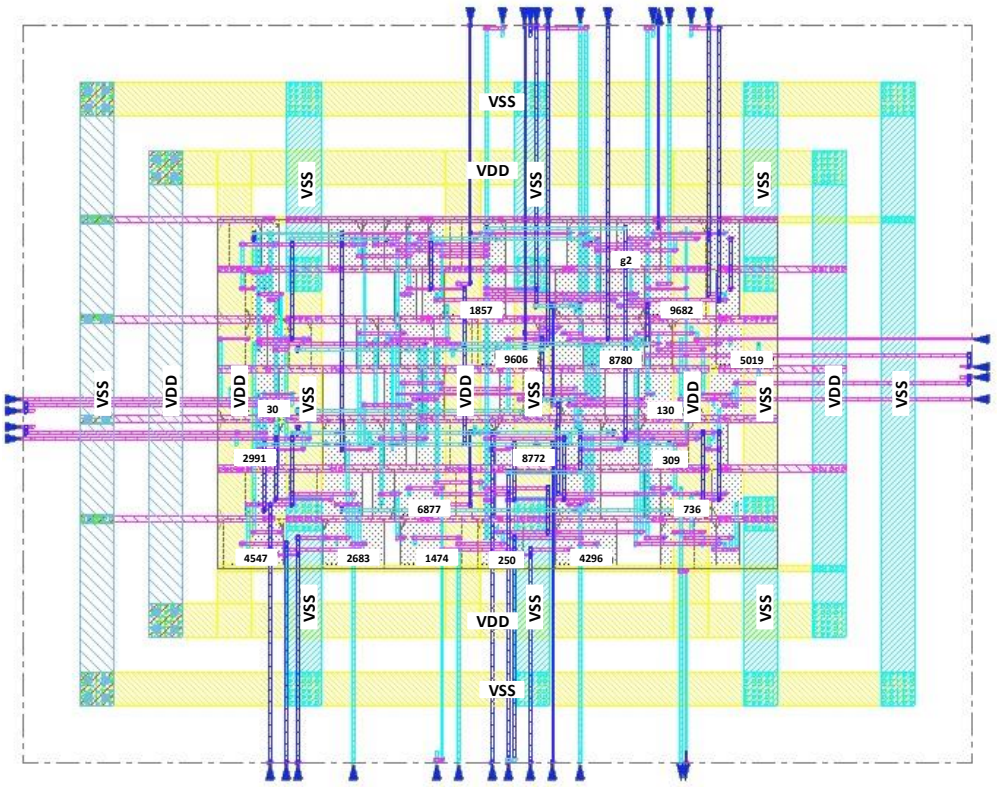


Fig. 7: The physical layout of the proposed 16-bit binary comparator using a 2-bit elementary comparator.

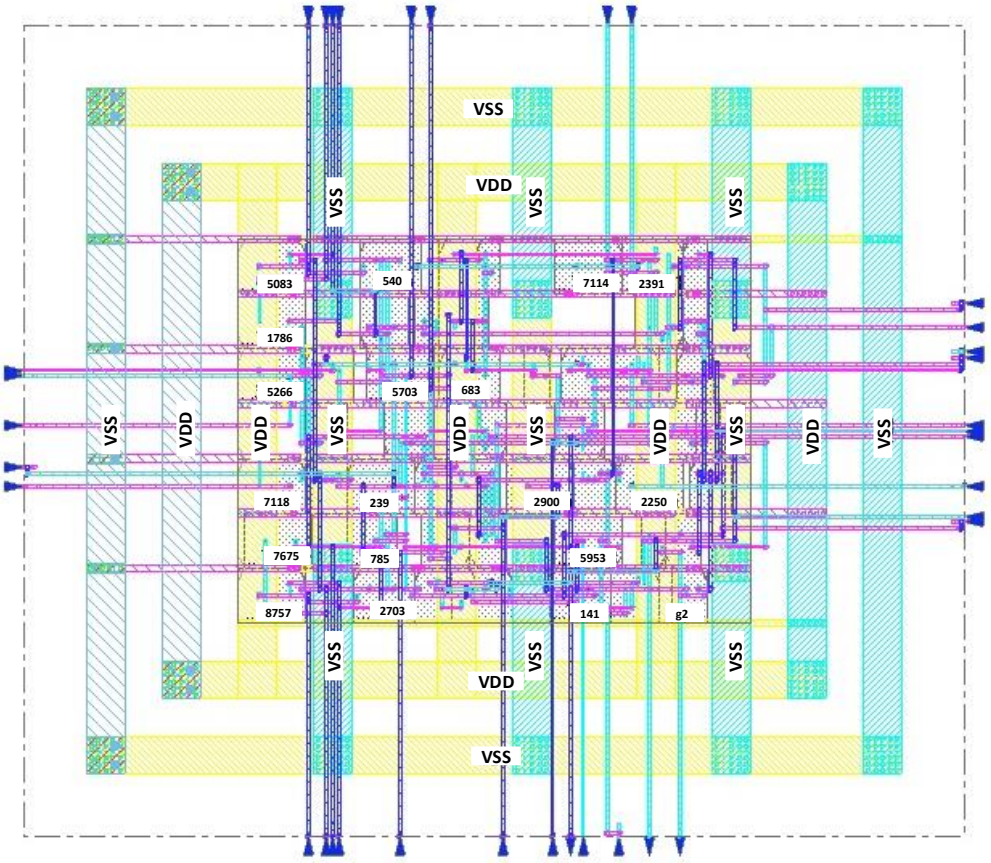


Fig. 8: The physical layout of the proposed 16-bit binary comparator using a 4-bit elementary comparator.

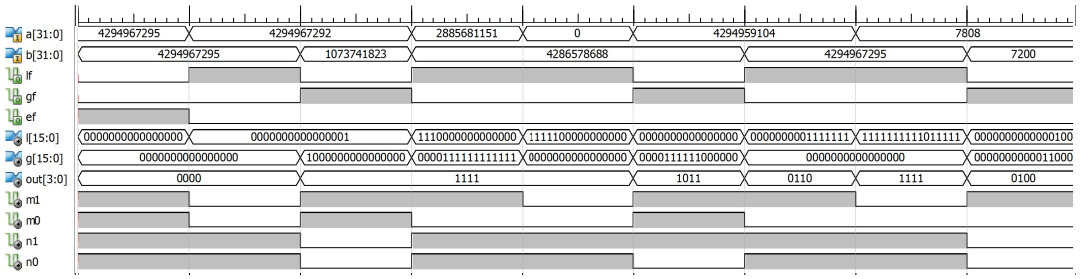


Fig. 9: Simulation waveform of the first proposed binary comparator circuit (32-bit).

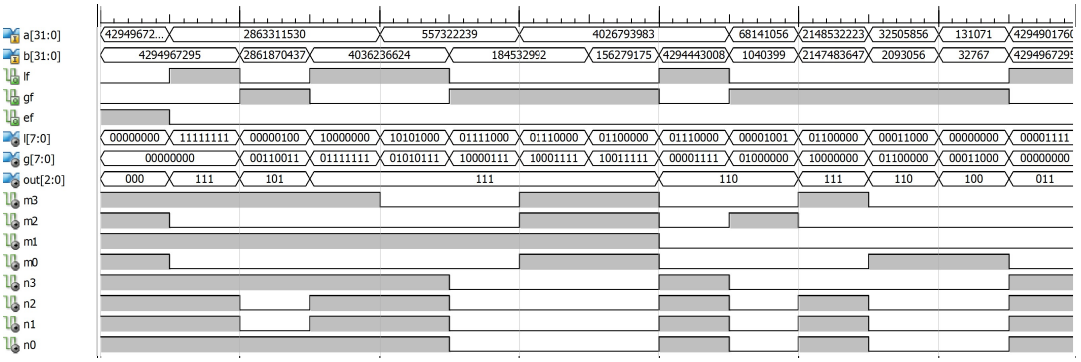
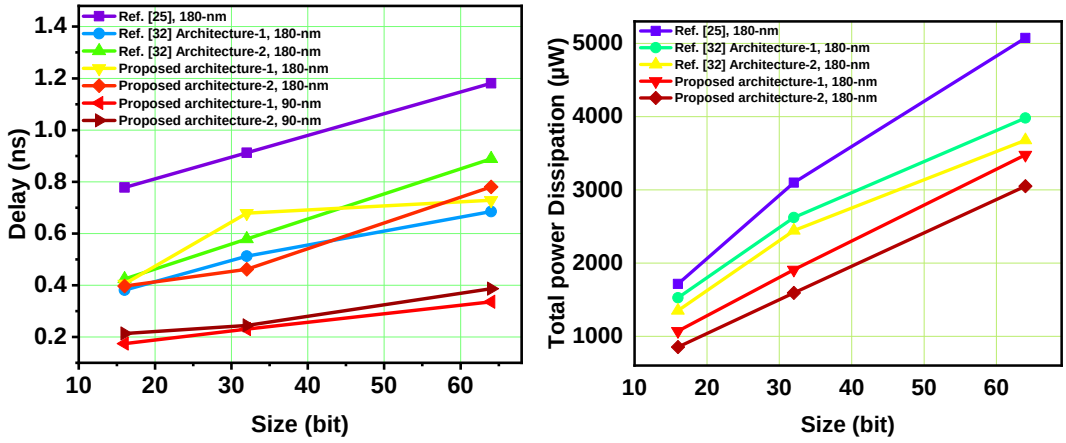
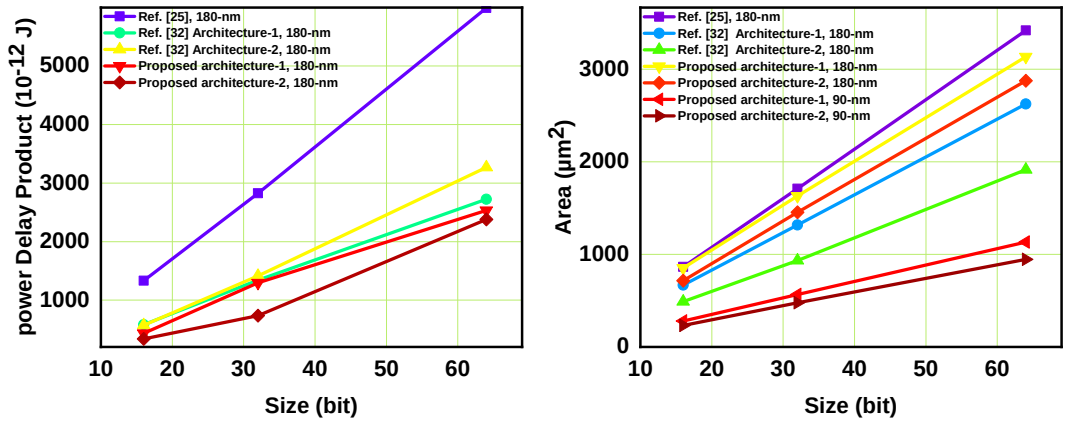


Fig. 10: Simulation waveform of second proposed architecture of binary comparator (32-bit).



(a) Delay.

(b) Total power dissipation.



(c) Power delay product.

(d) Chip area.

Fig. 11: Performance parameters of proposed and existing binary comparators.

32-bit operand size using the Verilog test bench is shown in Fig. 9 and Fig. 10. As presented in Fig. 9, the input operands a, b for 32-bit proposed binary comparator architecture-1 are presented. In the figure, lf, gf and ef represent "less", "greater" and "equal" output-bits of the proposed architecture. The intermediate signal l[15:0] and g[15:0] are 16-bit data corresponding to each 2-bit elementary comparator. The signal out[3:0] shows the output of 16 to 4-bit priority encoder. It's become a select line of four parallel 16 to 1 multiplexer and its outputs are given by M_1, M_0, N_1 and N_0. The 2-bit signal (M_1, M_0) and (N_1, N_0) become an input of the 2-bit binary comparator to get the final result i.e. lf, gf and ef. Similarly, in Fig. 10, the input operands a, b for 32-bit proposed binary comparator architecture-2 are presented. In the figure, lf, gf and ef represent "less", "greater" and "equal" output-bits of the proposed architecture. The intermediate signal l[8:0] and g[8:0] are 8-bit data corresponding to each 4-bit elementary comparator. The signal out[2:0] shows the output of 16 to 4-bit priority encoder. It's become a select line of eight parallel 8 to 1 multiplexer and its outputs are given by M_3, M_2, M_1, M_0, N_3, N_2, N_1 and N_0. The 4-bit signal (M_3, M_2, M_1, M_0) and (N_3, N_2, N_1, N_0) become an input of a 4-bit elementary binary comparator to get the final result.

The Power-Delay-Product (PDP) is the critical parameter for comparison today. The benchmarking based on PDP in Tab. 2 shows the superiority of the proposed design. As reported in Tab. 2, the proposed architecture-1 and 2 records 31.46 % and 39.89 %, respectively, less Power dissipation as compared to the existing literature [25]. Although the design proposed in [32] performs better in terms of delay alone when Power dissipation is taken into account, the proposed design is better by 12.63 % and 23.37 %, respectively and hence clearly outperforms both proposed architecture. As shown in Tab. 2, the proposed architecture-1 and 2 reduces PDP by 57.71 % and 60.26 %, respectively, as compared to the existing literature [25]. Although the design proposed in [32] performs better in terms of delay alone, when PDP is taken into account, the proposed architecture-1 and 2 is better by 22.46 % and 27.16 %, respectively.

The graphical representation of performance parameters in terms of delay, power dissipation, PDP, and chip area are shown in Fig. 11(a), Fig. 11(b), Fig. 11(c), and Fig. 11(d). Figure 11(a) shows the graph of critical path delay with different operands size of the binary comparator. One can observe from the plots that there is a small trade-off seen in the case of both proposed architectures with operands size. Whereas comparator [32] shows the higher trade-off as compared to proposed. The power dissipation for the proposed and existing architecture of binary comparator with different word lengths is shown in Fig. 11(b). One can observe from this figure that the total power consumption is getting reduced effectively when compared with existing literature. The plot of PDP versus operands size has been shown in Fig. 11(c) for the proposed and existing literature of binary comparator. It is demonstrating that both proposed architectures are superior in terms of PDP compared to the existing architecture. This plot also shows that the PDP of the proposed architecture is increased at a slower rate as compared to reported literature, as shown in the figure. Figure 11(d) shows the chip area versus operands size of the binary comparator. From this figure, it can be seen that the chip area of the proposed architectures is comparable to others. Detailed analysis reveals that it is the most power-efficient design. Finally, the proposed architectures are compared in terms of total power consumption, delay, PDP, and chip area as compared with existing literature of binary comparator. The main benefits of this design are its high speed and power efficiency maintained over a wide range of operands size, which is useful at low-input data activity environments. Therefore, the proposed architecture can be used to design modern processors or digital systems for low power and high speed applications.

6. Conclusion

A novel strategy for low-power binary comparator architecture design is presented in this work to achieve both low-power consumption and high-performance operation. The main advantage of this design is its high speed and power efficiency maintained over a wide range of operands size, which is useful at low-input data activity environments. This circuit design utilizes minimum fan-in and fan-out logic gates. The elementary 2-bit binary comparator is applied to design an architecture of parallel binary comparator for higher input operands by using low radix multiplexer and priority encoder. Further, to decrease the size of the multiplexer and priority encoder by two times, a general architecture is also proposed by using a 4-bit binary comparator to reduce its complexity. The proposed circuits are optimized in terms of power consumption and delay, which are due to low load capacitance, low leakages, and reduced dynamic power dissipation. Each of these circuits has its own merits in terms of speed, power consumption, and Power-Delay Product (PDP). The proposed comparators are also compared with some recently reported designs using identical technology. It is observed that the proposed design records the best result in terms of PDP, and it can be the design of choice in low-power, high-speed digital systems. The proposed architecture is validated using 180-nm CMOS technology. The overall PDP re-

duces by 22.46 % and 27.16 %, corresponding to each design (architecture-1 & -2) when compared to the earlier reported comparator circuit [32]. The proposed architecture can be used to design modern processors or digital systems for low power and high speed applications.

Author Contributions

M.D.G. and R.K.C. conceived of the presented idea. M.D.G. developed the theory and performed the computations. M.D.G. and R.K.C. verified the analytical methods. M.D.G. encouraged R.K.C. to investigate and supervised the findings of this work. All authors discussed the results and contributed to the final manuscript. M.D.G. wrote the paper in consultation with R.K.C. R.K.C. supervised the work.

References

[1] MUELLER, R., J. TEUBNER and G. ALONSO. Sorting networks on FPGAs. *The VLDB Journal*. 2012, vol. 21, iss. 1, pp. 1–23. ISSN 1066-8888. DOI: 10.1007/s00778-011-0232-z.

[2] CHENG, S.-W. Arbitrary long digit integer sorter HW/SW co-design. In: *Proceedings of the 2003 Asia and South Pacific Design Automation Conference*. Kitakyushu: ACM, 2003, pp. 538–543. ISBN 978-0-7803-7660-1. DOI: 10.1145/1119772.1119884.

[3] GUPTA, M. D. and R. K. CHAUHAN. Coupled variable-input LCG and clock divider-based large period pseudo-random bit generator on FPGA. *IET Computers & Digital Techniques*. 2021, vol. 15, iss. 3, pp. 1–13. ISSN 1751-861X. DOI: 10.1049/cdt2.12027.

[4] GUPTA, M. D. and R. K. CHAUHAN. Efficient Hardware Implementation of Pseudo-Random Bit Generator using Dual-CLCG Method. *Journal of Circuits, Systems and Computers*. 2020, ISSN 1793-6454. DOI: 10.1142/S0218126621501826.

[5] GONG, S., C. LIU, Y. JI, B. ZHONG, Y. LI and H. DONG. *Advanced Image and Video Processing Using MATLAB*. 1st ed. New York City: Springer, 2019. ISBN 978-3-319-77223-3.

[6] SA, P. K. and B. MAJHI. An improved adaptive impulsive noise suppression scheme for digital images. *AEU-International Journal of Electronics and Communications*. 2010, vol. 64, iss. 4, pp. 322–328. ISSN 1434-8411. DOI: 10.1016/j.aeue.2009.01.005.

[7] MEWADA, H. K. and J. CHAUDHARI. Low computation digital down converter using polyphase IIR filter. *Circuit World*. 2019, vol. 45, iss. 3, pp. 169–178. ISSN 0305-6120. DOI: 10.1108/CW-02-2019-0015.

[8] KIM, D., K. KIM, J.-Y. KIM, S. LEE and H.-J. YOO. An 81.6 GOPS Object Recognition Processor Based on NoC and Visual Image Processing Memory. In: *2007 IEEE Custom Integrated Circuits Conference*. San Jose: IEEE, 2007, pp. 443–446. ISBN 978-1-4244-0786-6. DOI: 10.1109/CICC.2007.4405769.

[9] LAZAROS, N., G. C. SIRAKOULIS and A. GASTERATOS. Review of Stereo Vision Algorithms: From Software to Hardware. *International Journal of Optomechatronics*. 2008, vol. 2, iss. 4, pp. 435–462. ISSN 1559-9612. DOI: 10.1080/15599610802438680.

[10] LOWE, D. G. Distinctive Image Features from Scale-Invariant Keypoints. *International Journal of Computer Vision*. 2004, vol. 60, iss. 2, pp. 91–110. ISSN 0920-5691. DOI: 10.1023/B:VISI.0000029664.99615.94.

[11] NAVABI. Z. *Digital System Test and Testable Design: Using HDL Models and Architectures*. 1st ed. New York City: Springer, 2011. ISBN 978-1-4419-7548-5.

[12] SHAHIDA, M. K. N., R. NORDIN and M. ISMAIL. An improved water-filling algorithm based on power allocation in network MIMO. *Telecommunication Systems*. 2020, vol. 75, iss. 4, pp. 447–460. ISSN 1018-4864. DOI: 10.1007/s11235-020-00695-5.

[13] WEY, I.-C., T.-C. HE, H.-C. CHOW, P.-H. SUN and C.-C. PENG. A high-speed, high fan-in dynamic comparator with low transistor count. *International Journal of Electronics*. 2014, vol. 101, iss. 5, pp. 681–690. ISSN 0020-7217. DOI: 10.1080/00207217.2013.794487.

[14] THEODORIDIS, G., S. THEOHARIS, D. SOUDRIS and C. GOUTIS. A Probabilistic Power Estimation Method for Combinational Circuits Under Real Gate Delay Model. *VLSI Design*. 2001, vol. 12, iss. 1, pp. 69–79. ISSN 1065-514X. DOI: 10.1155/2001/12026.

[15] GUANGJIE, W., S. SHIMIN and J. LIJIU. New efficient design of digital comparator. In: *2nd International Conference on ASIC*. Shanghai: IEEE, 1996, pp. 263–266. ISBN 7-5439-0940-5. DOI: 10.1109/ICASIC.1996.562803.

[16] KYTHE, D. K. and P. K. KYTHE. *Algebraic and stochastic coding theory*. 1st ed. Boca Raton: CRC Press 2012. ISBN 978-1-4398-8181-1.

[17] HENSLEY, J., M. SINGH and A. LASTRA. A fast, energy-efficient z-comparator. In: *Proceedings of the ACM SIGGRAPH/EUROGRAPHICS Conference on Graphics Hardware*. Los Angeles: ACM Press, 2005, pp. 41–44. ISBN 978-1-59593-086-6. DOI: 10.1145/1071866.1071873.

[18] MUKHERJEE, D. N., S. PANDA and B. MAJI. Performance Evaluation of Digital Comparator Using Different Logic Styles. *IETE Journal of Research*. 2018, vol. 64, iss. 3, pp. 422–429. ISSN 0377-2063. DOI: 10.1080/03772063.2017.1323564.

[19] MUKHERJEE, D. N., S. PANDA and B. MAJI. A Novel Design of 12-bit Digital Comparator Using Multiplexer for High Speed Application in 32-nm CMOS Technology. *IETE Journal of Research*. 2019, vol. 65, iss. 1, pp. 1–8. ISSN 0377-2063. DOI: 10.1080/03772063.2019.1649204.

[20] WANG, C.-C., C.-F. WU and K.-C. TSAI. 1 GHz 64-bit high-speed comparator using ANT dynamic logic with two-phase clocking. *IEE Proceedings-Computers and Digital Techniques*. 1998, vol. 145, iss. 6, pp. 433–436. ISSN 1359-7027. DOI: 10.1049/ip-cdt:19982348.

[21] HUANG, C.-H. and J.-S. WANG. High-performance and power-efficient CMOS comparators. *IEEE Journal of Solid-State Circuits*. 2003, vol. 38, iss. 2, pp. 254–262. ISSN 1558-173X. DOI: 10.1109/JSSC.2002.807409.

[22] LAM, H.-M. and C.-Y. TSUI. High-performance single clock cycle CMOS comparator. *Electronics Letters*. 2006, vol. 42, iss. 2, pp. 75–77. ISSN 1350-911X. DOI: 10.1049/el:20063083.

[23] KIM, J. Y. and H. J. YOO. Bitwise Competition Logic for compact digital comparator. In: *2007 IEEE Asian Solid-State Circuits Conference*. Jeju: IEEE, 2007, pp. 59–62. ISBN 978-1-4244-1359-1. DOI: 10.1109/ASSCC.2007.4425682.

[24] GUPTA, R., R. GUPTA and S. SHARMA. Design of high speed and low power 4-bit comparator using FGMOS. *AEU-International Journal of Electronics and Communications*. 2017, vol. 76, iss. 1, pp. 125–131. ISSN 1434-8411. DOI: 10.1016/j.aeue.2017.04.004.

[25] ABDEL-HAFEEZ, S., A. GORDON-ROSS and B. PARHAMI. Scalable Digital CMOS Comparator Using a Parallel Prefix Tree. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 2012, vol. 21, iss. 11, pp. 1989–1998. ISSN 1557-9999. DOI: 10.1109/TVLSI.2012.2222453.

[26] FURUYA, K. Design methodologies of comparators based on parallel hardware algorithms. In: *2010 10th International Symposium on Communications and Information Technologies*. Tokyo: IEEE, 2010, pp. 591–596. ISBN 978-1-4244-7010-5. DOI: 10.1109/ISCIT.2010.5665060.

[27] VEERAMACHANENI, S., M. K. KRISHNA, L. AVINASH, R. P. SREEKANTH and M. B. SRINIVAS. Efficient design of 32-bit comparator using carry look-ahead logic. In: *2007 IEEE Northeast Workshop on Circuits and Systems*. Montreal: IEEE, 2007, pp. 867–870. ISBN 978-1-4244-1163-4. DOI: 10.1109/NEWCAS.2007.4487986.

[28] PERRI, S. and P. CORSONELLO. Fast Low-Cost Implementation of Single-Clock-Cycle Binary Comparator. *IEEE Transactions on Circuits and Systems II: Express Briefs*. 2008, vol. 55, iss. 12, pp. 1239–1243. ISSN 1558-3791. DOI: 10.1109/TCSII.2008.2008063.

[29] FRUSTACI, F., S. PERRI, M. LANUZZA and P. CORSONELLO. A new low-power high-speed single-clock-cycle binary comparator. In: *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*. Paris: IEEE, 2010, pp. 317–320. ISBN 978-1-4244-5308-5. DOI: 10.1109/ISCAS.2010.5537827.

[30] CHUANG, P., D. LI and M. SACHDEV. A Low-Power High-Performance Single-Cycle Tree-Based 64-Bit Binary Comparator. *IEEE Transactions on Circuits and Systems II: Express Briefs*. 2012, vol. 59, iss. 2, pp. 108–112. ISSN 1558-3791. DOI: 10.1109/TCSII.2011.2180110.

[31] CHUANG, P. I.-J., M. SACHDEV and V. C. GAUDET. A 167-ps 2.34-mW Single-Cycle 64-Bit Binary Tree Comparator With Constant-Delay Logic in 65-nm CMOS. *IEEE Transactions on Circuits and Systems I: Regular Papers*. 2013, vol. 61, iss. 1, pp. 160–171. ISSN 1558-0806. DOI: 10.1109/TCSI.2013.2268591.

[32] CHUA, C., R. B. N. KUMAR and B. SIREESHA. Design and analysis of low-power and area efficient N-bit parallel binary comparator. *Analog Integrated Circuits and Signal Processing*. 2017, vol. 92, iss. 2, pp. 225–231. ISSN 0925-1030. DOI: 10.1007/s10470-017-0996-1.

[33] GUPTA, M. D. and R. K. CHAUHAN. Accurate Estimation of Power Consumption for Binary Comparator System using Back Tracking. *ECTI*

Transactions on Electrical Engineering, Electronics, and Communications. 2021, vol. 19, iss. 2. ISSN 1685-9545.

[34] Cadence Online Documentation. In: *Cadence* [online]. 2021. Available at: https://www.cadence.com/en_US/home.html.

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